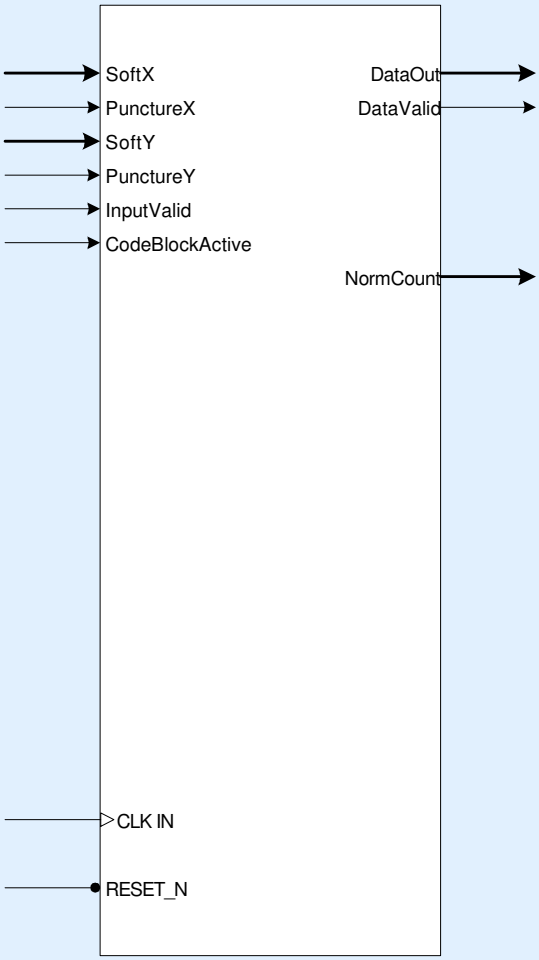
(Burst-mode) Viterbi Decoder

CMS0002

- Programmable constraint length.
- Programmable generator coefficients.
- Supports variable puncture rates. External logic provides puncture pattern. Internal logic calculates modified branch metrics.
- Zero-flush mode for 802.11a.
- Continuous mode for DOCSIS, DVB-T and many other applications.
- Configurable traceback length.
- Configurable soft-decision width.
- Flexible memory architecture suitable for FPGA or ASIC.



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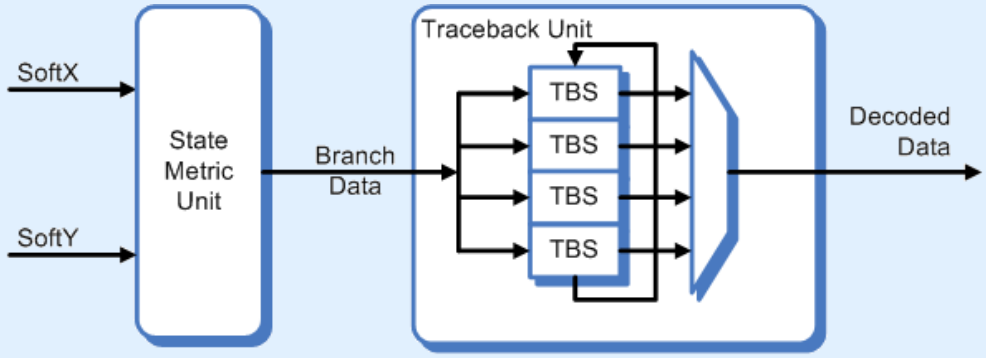
Block Diagram



Detailed Description

The Commsonic CMS0002 Viterbi Decoder core implements Viterbi's algorithm for maximum likelihood decoding of non-feedback convolutional codes. Applications include DOCSIS (J.83B), DVB-T, 802.11a and 802.16.

The basic 1/2 rate convolutional encoder and decoder are shown above. For each input bit, two encoded bits are produced. The rate can be increased to 2/3, 3/4, 5/6, or 7/8 by non-transmission (puncture) of certain bits. Punctured codes lose coding gain as the redundant content decreases.

The encoded X and Y bits are transmitted through a noisy channel. The received X and Y values are measured then presented as soft decision values to the decoder.

A description of the processing steps follows:

State Metric Unit. This block maintains a measure of probability for each possible encoder state. As each soft pair is processed, the SMU produces the most likely received data bit for each state (the Branch Data vector).

Traceback Unit. This block provides a history of most likely state transitions. This allows traceback from any current state to ever more likely predecessor states. After a certain depth the optimum state becomes known and traceback from this point produces reliable data. The required minimum traceback depth depends on the code parameters, puncture rate and soft-decision width.

Zero Flush

Both 802.11a and 802.16 specify this mode of operation. With this approach, the convolutional encoder is guaranteed to be in state zero at both the beginning and end of the burst. This is especially important at the end of the burst because there is no further history to trace back from.

To support this mode, state metrics are initialised at the beginning of the burst such that all possible successor states will ultimately be based on state 0.

At the end of the burst, extra zeros are appended to the data stream to flush the encoder to its known final state of 0. The known final state gives a valid starting point for traceback in the decoder.

When the CodeBlockActive input goes to zero, the decoder forces a final state of zero and begins traceback of the data.

Detailed Description (Cont'd)

Memory Configuration

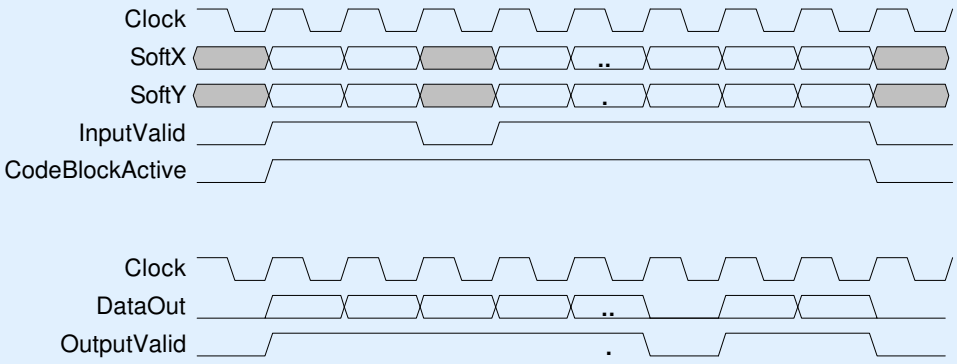
The core uses a novel memory architecture for the Traceback Unit. Traceback is performed in chunks of configurable size. These are arranged in a ring with each slice receiving a Best End State and producing a Best Initial State. The number of traceback slices (TBS) varies depending on ChunkSize and TBlength.

This allows separate optimisation for FPGA or ASIC. Often ASIC memory has a large minimum size (e.g. 64 words) with each RAM cell requiring individual attention and consequently a small number of larger RAM cells are appropriate.

Conversely, for FPGA applications, RAMs may be built from logic cells and the total bit count may be minimised by using a larger number of small RAM cells.

Note, that the total group delay through the decoder is reduced by using smaller ChunkSize. Refer to the Synthesis Controls section for further information.

Decoder Timing Diagram



Notes,

1. Data is transferred on cycles when InputValid = 1.
2. Data is transferred out on cycles when OutputValid = 1.
3. If InputValid is continuous and equal to CodeBlockActive, OutputValid will be continuous.
4. Voids (null cycles) in the input stream will cause voids in the output stream.

Principle I/O Description

Datapath Inputs	
SoftX	X and Y decoder soft decision inputs. 0000 => strong 0, 1111 => strong 1
SoftY	
PunctureX	These signals indicate that the corresponding SoftX or SoftY input has been punctured from the code. The state metric unit removes that soft decision from the maximum-likelihood calculation. External logic must provide the puncture pattern.
PunctureY	
InputValid	Indicates clock cycle on which soft data and puncture inputs are valid.
Frame Control	
CodeBlockActive	Frames active code block. Must be continuously high for all input cycles in a code block. When the code block size is a multiple of ChunkSize, the minimum low time between code blocks is one clock cycle. For other sizes of code block, see the detailed design documentation for calculation of Burst Recovery time.
Outputs	
DataOut	Decoded data
DataValid	Indicates clock cycle on which decoded data is valid
Status Output	
NormCount	Counts normalization events. The rate of change provides an indicator of noise level.

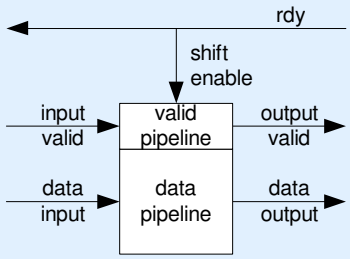
Synthesis Controls

ConstraintLength	Constraint length of the convolutional code = log2(states)+1 = state_shift_register_length+1
Gx	Defines convolutional encoder x output as function of state
Gy	Defines convolutional encoder y output as function of state
SoftLength	Soft decision inputs range from 0 to $2^{SoftLength}$-1
TBlength	Minimum traceback required; must be a multiple of chunk size
ChunkSize	The number of RAM words in each traceback slice (chunk). The following table shows the effect of chunk size selection for a typical traceback length.
NumChunks	0 => The default number of chunks is calculated based on maximum bit-per-clock output, as show in the table above. If used with lower data rates, the core may be synthesised with fewer chunks. If soft-decision pairs are presented at clock/n, then NumChunks = (TBlength + ChunkSize) * (1 + 1/n) / ChunkSize

Traceback Length	ChunkSize	Number of Chunks	Total RAM	Traceback Delay
96	96	4	384	384
96	48	6	288	288
96	32	8	256	256
96	16	14	224	224

Encoder Operation

To support bi-directional flow control, the encoder block implements bi-directional handshaking signals. Data transfer occurs on clock cycles when both Rdy and Ack are valid. Rdy must be true to fill the pipeline.



Datapath Inputs	
DataIn	Uncoded input data bits
Dataflow Control	
InputValid	Input indicating clock cycle on which data input is valid
Rdy	Input indicating next block is ready to accept encoded output data
OutputValid	Output indicating clock cycle on which encoded data outputs are valid
Frame Control	
BurstActive	Frames active code block. Must be continuously high for all input cycles in a co block.
Datapath Outputs	
Xout	X and Y encoder outputs
Yout	

Synthesis Controls

ConstraintLength	Constraint length of the convolutional code = log2(states)+1 = state_shift_register_length+1
Gx	Defines convolutional encoder x output as function of state
Gy	Defines convolutional encoder y output as function of state

About Commsonic:

Commsonic is an IP and design services company that specialises in the development of ASIC, FPGA, DSP and board-level sub-systems for applications in wireless and wireline communications.

Our expertise is primarily in the gate- and power-efficient implementation of physical-layer (PHY) functions such as modulation, demodulation and channel coding, but we have extensive experience with all of the major elements of a modern baseband 'core' including medium access control (MAC), voiceband DSP, mixed-signal interfaces and embedded CPU and software.

Our services are available on a turn-key basis but they are usually provided as part of a support package attached to members of our expanding family of licensable IP cores.

Commsonic's IP spans the major Standards for cable, satellite and terrestrial digital TV transmission and includes high-performance, adaptable, single-carrier (QAM) and multi-carrier (COFDM) modulator and demodulator solutions for DVB-S2, DVB-C/J.83/A/B/C and DVB-T/H.

Commsonic's customers are typically semiconductor vendors and manufacturers of broadband transceiver equipment that demand leading-edge Standards-based or proprietary PHY solutions but don't have the internal resources necessary to get their products to market soon enough.

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